

REMARKS

Claims 1-5 and 11-24 are pending, with claims 1, 13, and 18 being independent. Claims 6-10, which were withdrawn due to a restriction requirement, are cancelled by this amendment without waiver or prejudice. New claims 11-24 are added by this amendment. No new matter is added.

Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Agarwal (U.S. Patent No. 6,308,252). Applicants have amended independent claim 1 to obviate this rejection.

As amended, claim 1 recites a digital signal processor that includes two execution pipelines capable of executing RISC and DSP instructions, instruction fetch logic that simultaneously fetches two instructions and routes them to respective pipelines, and control logic to allow the pipelines to operate independently. This amendment is supported in the specification and drawings, for example, in Figure 9 that illustrates two pipes, Pipe A and Pipe B, where Pipe A is capable of executing RISC instructions (e.g., the first column of the MIPS 32-bit general instructions block) and DSP instructions (e.g., the first column of the LEXRA Vector Addressing block) and Pipe B is capable of executing RISC instructions (e.g., the second column of the MIPS 32-bit general instructions block) and DSP instructions (e.g., the second column of the LEXRA MAC Instructions block).

Applicants respectfully request reconsideration and withdrawal of the rejection because Agarwal does not describe or suggest two execution pipelines capable of executing RISC and DSP instructions. Instead, Agarwal describes pipelines that are only capable of executing RISC instructions. Agarwal does not describe a digital signal processor that includes two execution pipelines that are capable of executing RISC and DSP instructions.

For at least these reasons, applicants respectfully request reconsideration and withdrawal of the rejection of amended independent claim 1 and its dependent claims 2 and 3.

Claims 4 and 5, which depend from amended claim 1, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Agarwal in view of Chuang (U.S. Patent No. 4,766,566). Applicants respectfully request reconsideration and withdrawal of the rejection because Chuang

does not remedy the failure of Agarwal to describe or suggest a digital signal processor that includes two execution pipelines that are capable of executing RISC and DSP instructions, as recited in amended claim 1, from which claims 4 and 5 depend.

New independent claim 13 recites a method for processing instructions in a digital signal processor that includes simultaneously fetching a first instruction and a second instruction and routing the first instruction to a first execution pipeline and the second instruction to a second execution pipeline, where the first execution pipeline and the second execution pipeline are capable of executing RISC and DSP instructions. Control logic is used to operate the first execution pipeline and the second execution pipeline independently.

New independent claim 18 recites a system for processing instructions that an instruction memory having instructions and a digital signal processor that includes two execution pipelines capable of executing RISC and DSP instructions. The digital signal processor includes instruction fetch logic that simultaneously fetches two instructions from the instruction memory and routes them to respective pipelines and control logic to allow the pipelines to operate independently.

Applicants submit that independent claims 13 and 18, and their respective dependent claims 14-17 and 19-24, are in condition for allowance over the cited prior art at least for the reasons discussed above with respect to claim 1.

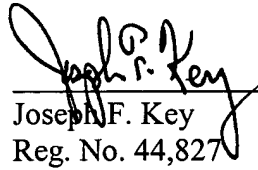
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Enclosed is a \$1020 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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